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Abstract
In the last decade, discrete wavelet transform (DWT) has proven to be a useful technique for a wide range of applications including signal analysis, signal compression, pattern recognition, biomedicine, and numerical analysis. Since DWT has excellent features of energy compaction and inherent scalability, it has been applied extensively in the field of image and video compression.

In 1996, lifting-based discrete wavelet transform (LDWT) is proposed. With some advantages, such as lower implementation complexity and easy VLSI implementation, LDWT has received considerable attention recently. In this paper, we propose an efficient VLSI architecture for 1-D LDWT, and its FPGA implementation. The architecture folds the computations of all resolution levels into the same low-pass and high-pass units to achieve higher hardware utilization. Because of its modular, regular and flexible structure, the design is scalable for different resolution levels. The number of registers in the folded architecture is minimized by using time scheduling and register allocation. Since the architecture has the similar topology of a scan chain, we can modify it easily to become a testable scan path design by adding very few hardware resources.

In the first part, we present two different 1-D multi-level LDWT architectures by using 5/3 and 9/7 filters, respectively. Those architectures are suitable for 1-D DWT processing, such as speech compression. In the second part, we present a low-cost and high-utilization folded architecture for 2-D 3-level LDWT. The architecture can be used in 2-D digital image processing, such as JPEG2000 image compression standard.

All proposed VLSI architectures are realized with verilog HDL, synthesized by the synopsys Design Compiler. Finally, the layouts for those designs are generated with the Avant! Apollo Tools in a 0.35um 1P4M CMOS technology.
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